Breakdown Ruggedness of Quasi-Vertical GaN-Based p-i-n Diodes on Si Substrates

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***Abstract*— This letter reports the breakdown ruggedness of GaN-based quasi-vertical p-i-n diodes on Si for the first time. With a 2-μm-thick drift layer, the 0.08-mm^2 devices can sustain a surge current up to 0.73 A, and maximum sink in energy of 3 mJ using an unclamped inductive switching test setup. No parametric drift nor device degradation was found after repetitive avalanche test consisting of multiple 50 000 breakdown events with a frequency of 1 kHz. At elevated temperatures, the breakdown voltage exhibits little temperature dependence, which could be explained by a trap-assisted space-charge-limited current conduction mechanism. With good ruggedness quality under repetitive test and at elevated temperatures, the quasi-vertical GaN p-i-n diodes on Si show great potential in achieving cost-effective rectifiers for high-voltage applications.**

***Index Terms*— GaN-on-Si, p-i-n diodes, rectifiers, breakdown ruggedness.**

I. Introduction

THE outstanding material properties of III-nitride semiconductors such as wide bandgap, large critical electrical field, and good thermal dissipation capability have spurred extensive research efforts in developing GaN-based optoelectronic and electronic devices for lighting, high frequency and high power applications [1]–[3]. With the continuous progress in GaN material epitaxial growth, GaN-on-Si epilayers have been investigated extensively for various devices due to their low cost, large size availability, and integration potential with Si-based circuits [4], [5]. Light-emitting diodes (LEDs) [6]–[8], Schottky barrier diodes (SBD) [9], and high electron mobility transistors (HEMTs) [10], [11] have been demonstrated using GaN-on-Si epilayers.

With the success of GaN-on-Si, there have been research efforts in developing p-i-n diodes using GaN-on-Si epilayers [9], [12]–[14]. Diode characteristics and device technologies have been reported for achieving inexpensive GaN-on-Si vertical diodes. For some applications, such as power supply, rectification, and transient voltage suppression, it is important and critical to know the diodes' breakdown ruggedness. Avalanche breakdown capability has been reported recently for GaN-on-GaN vertical diodes [15], [16]. The breakdown ruggedness and reliability performance for GaN p-i-n diodes on mismatched Si substrates remain unexplored and it is essential and valuable information for future device development.

In this letter, we demonstrate, for the first time, the breakdown ruggedness of quasi-vertical GaN-based p-i-n diodes on original growth Si (111) substrate using an unclamped inductive switching (UIS) test setup. With a 2-μm-thick drift layer, the diodes can sustain surge currents up to 0.73 A, reverse voltages of 507 V, and maximum sink in energy of 3 mJ. The devices also demonstrated good ruggedness quality in repetitive test and at elevated temperatures, indicating the great potential of GaN p-i-n diodes on Si for high voltage applications.

II. Device Structure and Measurement Set-Up

Fig. 1 (a) shows a schematic of a quasi-vertical p-i-n diode grown on a Si (111) substrate. The p-i-n structure on Si started from a 1.2-μm thick graded AlGaN buffer, and followed by an 800-nm thick Si-doped n-GaN layer ($\sim$n $= 2 \times 10^{18}$ cm^{-3}), a 2-μm thick undoped i-GaN layer (carrier concentration at the order of 10^{16} cm^{-3}), and a 500-nm thick Mg-doped p-type GaN ($\sim$p $= 2 \times 10^{17}$ cm^{-3}). The device fabrication process began with mesa etching to expose the n-GaN using dry etching. A 5 nm/5 nm Ni/Au stack was deposited and annealed to form ohmic contacts to the p-GaN. Subsequently, a SiO_2 layer was deposited by plasma enhanced chemical vapor deposition (PECVD) for device sidewall passivation and the quasi-vertical device was finished by depositing Cr/Al-based metal as electrodes.

To test the breakdown ruggedness of the diodes, an UIS test setup [16]–[18] was employed as shown in Fig. 2. One SiC metal-oxide-semiconductor transistor with a breakdown voltage of 1700 V was first turned on to allow the inductor current build up linearly. After the current reached the preconfigured value, the SiC transistor was turned off. The current was then forced into the reverse direction of the diode under test (DUT). By controlling the SiC transistor gate through an external pulse generator, single pulse test or repetitive pulse test can be performed to drive the diode into breakdown once-only or consecutively. The temperature

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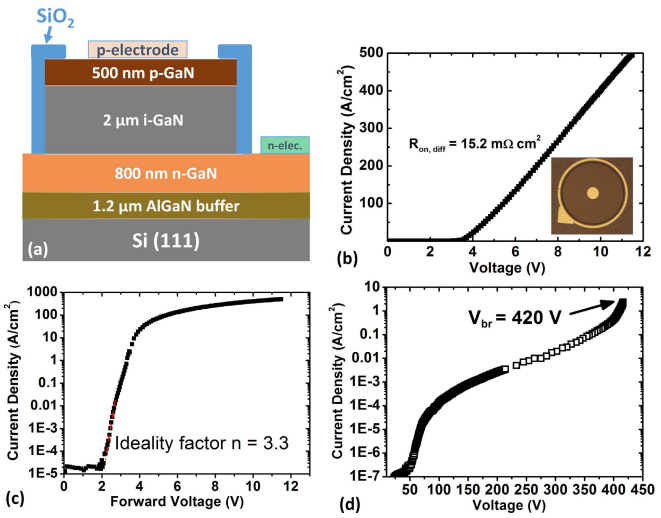

Fig. 1. (a) Schematic cross section of quasi-vertical p-i-n diodes on original Si (111) growth substrates; (b,c) Forward I-V characteristics in linear and semi-log scale; (d) Reverse I-V characteristics.

dependent measurements were conducted by attaching the devices on a hot surface with temperature monitored by a thermometer.

III. Results and Discussion

Fig. 1 (b, c) shows the forward I-V characteristics of a 0.08 mm^2 GaN quasi-vertical p-i-n diode. A turn-on voltage of 3.4 V can be extracted at 1 A/cm^2 and an ideality factor of 3.3 was obtained. The differential on-resistance $R_{on,diff}$ was calculated to be 15.2 $m\Omega \cdot cm^2$ after turn-on. The reverse characteristic is plotted in Fig. 1 (d). With SiO_2 sidewall passivation, the leakage current density at 200 V was measured to be $(4 \pm 1) \times 10^{-3}$ A/cm^2, which is comparable with p-i-n diodes on foreign substrates reported elsewhere [9], [14], [19], [20]. Reverse breakdown of the diode was observed at 420 V bias, leading to a Baliga figure of merit (FOM) of 11.60 MW/cm^2. The reverse current increased rapidly when the bias approached breakdown voltage near 420 V but the diode showed good robustness without destruction when the bias moved beyond and back near the breakdown voltage even under DC bias.

Using the circuit in Fig.2 and a 5 mH load inductor (L), a captured waveform for the 0.08 mm^2 diode in the single pulse breakdown condition is shown in Fig. 3. The diode could sustain a single peak surge current I_{RM} as high as 730 mA. The reverse voltage of the diode at the peak current was measured to be 507 V. Given that the reverse bias was mainly sustained by the 2 μm-thick i-GaN drift layer in the structure, the average electrical field that was exerted on the GaN was calculated to be 2.5 MV/cm, which was comparable to the reported highest value (2.9 MV/cm) for GaN devices on Si substrates [9]. Table I summarizes representative pulse parameters that the device can sustain using three different inductors. With a larger inductor, the diode breakdown period could be extended to push up the total energy absorbed by the diode. Under a 40 mH load inductor, when a surge current of 400 mA was introduced, a breakdown period of 30 μs was achieved, leading to an absorbed energy as high as 3.0 mJ for the GaN diode on Si without destruction.

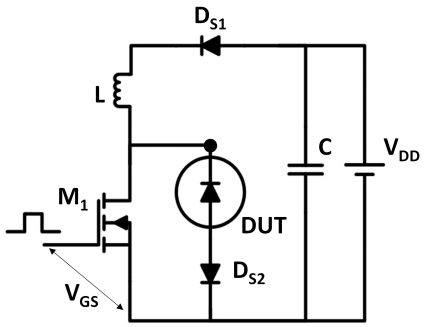

Fig. 2. Breakdown ruggedness test circuit. D_{S1} and D_{S2} are two Schottky diodes. M_1 is SiC metal-oxide-semiconductor transistor as a switch.

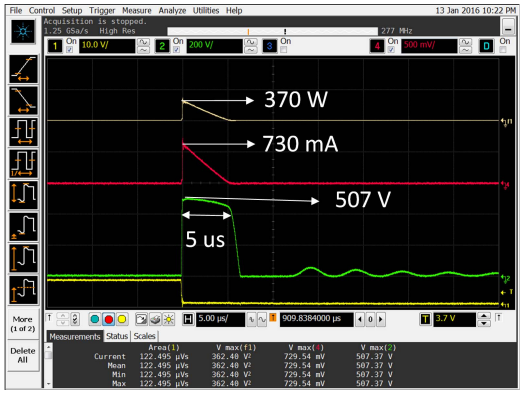

Fig. 3. Waveform captured from the oscilloscope screen using a 5 mH inductor.

TABLE I
Summary of the Representative Pulse Parameters That the Device Can Sustain Using Three Different Inductors

Inductor used	Peak Current	Peak Voltage	Duration	Sink in Energy
5 mH	730 mA	507 V	5 μs	1.1 mJ
9 mH	680 mA	505 V	12 μs	2.0 mJ
40 mH	400 mA	492 V	30 μs	3.0 mJ

The device was further tested in a three-step stress setup with each step consisting of 50,000 times breakdown with a switching frequency of 1k-Hz at a certain stressing current. In the stepwise stress test, the stressing current peak was initially set as 145 mA (Step 1: 20% of I_{RM}), then increased to 295 mA (Step 2: 40 % of I_{RM}), and 410 mA (Step 3: 56% of I_{RM}). There was a minimum of 5 minutes between each step test. The forward and reverse I-V characteristics of the diodes before and after the test were plotted in Fig. 4. No parametric drift nor device degradation was found for the diodes after the step-stress test, which indicated good ruggedness quality of the p-i-n diodes on Si for repetitive usage. Most of the diodes could survive the above three-step test. For those passing the three-step stressing, two extra 50,000 times repetitive test with avalanche current of 410 mA was conducted. The fact that around half of the diodes survived showed good avalanche capability of the p-i-n diodes grown on Si substrates. It was also found that another batch of diodes with similar reverse I-V characteristics but somewhat larger $R_{on,diff}$ (39.1 $m\Omega \cdot cm^2$) exhibited a high failure rate in the repetitive stressing test, even the stressing current was set as a low level of 295 mA. A burn hole could be observed in

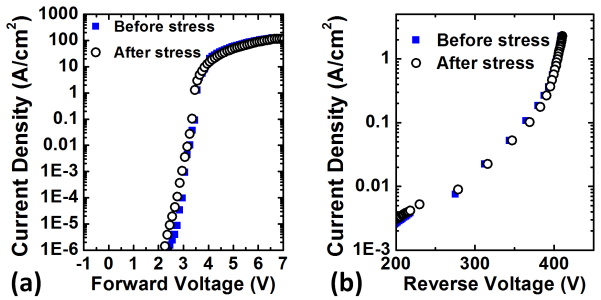

Fig. 4. (a) Forward and (b) reverse I-V characteristics of the diodes on Si before and after the three-step stress test.

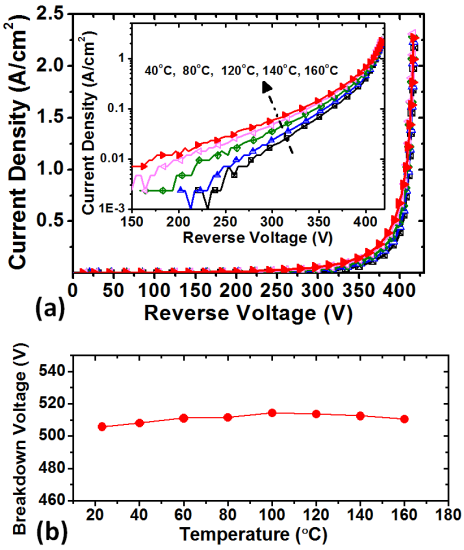

Fig. 5. (a) Reverse I-V characteristic of the diodes at elevated temperatures under DC bias; (b) Distribution of reverse voltages at 400 mA avalanche current at elevated temperatures using UIS setup.

the Ni/Au stack of the burnt diode, suggesting the destruction was induced by overheating associated with the large contact resistance between the p-metal and p-GaN.

Fig. 5 shows the temperature dependent test results of the quasi-vertical diodes on Si. Fig.5 (a) shows the reverse I-V characteristics under DC conditions at temperatures from 40 °C to 160 °C. From the graph, the evolvement of the reverse current can be divided into two stages. When the reverse voltage was smaller than 300 V, the natural logarithm of the reverse current *(ln(I))* was linear to the bias at all temperature steps, indicating the reverse current was limited by variable-range hopping (VRH) [12], [21] which was thought to be related to the dislocations in the GaN-on-Si.

As the reverse bias was increased to over 300 V, trap-assisted space-charge-limited current (SCLC) [9], [13], [22] started to dominate the leakage current. In the 300 - 400V regime, the current density could be modeled by $I \sim V^n$, where n was calculated to be in the range of 6 to 11, suggesting de-ionization of donor traps. As the reverse bias was approaching the breakdown voltage 420 V, the current began to increase at a dramatically faster rate (n could be as large as 40 if using $I \sim V^n$ to fit the curve), indicating generation of more free electrons in the conduction band and on-set of a pure drift process.

Although the reverse current increased slightly with the temperatures at relatively small reverse bias, the diodes showed

TABLE II

BREAKDOWN RUGGEDNESS COMPARISON OF SiC ABD, GaN-ON-GaN VERTICAL p-i-n DIODES, AND GaN-ON-Si QUASI-VERTICAL DIODES

Diode Information	Surge current (Density)	Surge voltage	Electric field	Sink in energy
SiC ABD [18]	104 A (1.16 kA/cm^2)	1110 V	--	--
GaN-on-GaN vertical diodes [16]	10 A (2.8 kA/cm^2)	1100 V	3.3 MV/cm	10 mJ
GaN-on-Si diodes (This work)	0.73 A (0.91 kA/ cm^2)	510 V	2.5 MV/cm	3.0 mJ

the same breakdown voltage of 420 V at temperatures from 40 °C to 160 °C at DC conditions. Moreover, under UIS test (using a 5 mH inductor), the diodes also exhibited almost the same reverse voltage of 510 V at 400 mA avalanche current regardless of the measurement temperatures up to 160 °C. This is consistent with the observation in Fig. 3 that during the 5 μs breakdown period, the device voltage remained nearly steady as the energy was deposited on the device and junction temperature was increased. The temperature-insensitive property was different from what was reported in Ref. [16] that the device voltage exhibited a gradual increase due to heat or increased temperature.

The steady breakdown voltage in our quasi-vertical diode on Si further confirmed trap-assisted SCLC as the conduction mechanism of the diode under large electrical field. As reported by Zhou *et al.* [22], the vertical breakdown voltage of a GaN layer is associated with its acceptor/donor trap numbers with no temperature dependence. The temperature-independent breakdown voltage of our p-i-n diodes guarantees high reliability at elevated temperatures and could facilitate usage of the diode without serious concerns of junction temperatures.

The ruggedness characteristics are also benchmarked with SiC avalanche breakdown diodes (ABD) and GaN-on-GaN vertical diodes, as summarized in Table II. This work presents p-i-n diodes using GaN-on-Si epitaxial layers with reasonably high surge current density and average electrical field. Given the low cost and large size availability of Si growth substrate, the GaN p-i-n diodes on Si show promising potential to realize cost-effective high-voltage rectifiers.

IV. CONCLUSIONS

GaN-based quasi-vertical p-i-n diodes on Si were fabricated and their breakdown ruggedness was characterized using both DC bias and a UIS test setup. With 2-μm-thick drift layer, the 0.08 mm^2 devices demonstrated a $R_{on,diff}$ of 15.2 m$\Omega \cdot$cm^2 and a breakdown voltage of 420 V under DC bias. Using a UIS set up, the diode can sustain a surge current up to 0.73 A, average electrical field of 2.5 MV/cm, and a maximum sink in energy of 3 mJ in a single pulse avalanche. The diodes could also survive multi 50,000 breakdown cycles with a frequency of 1k-Hz, demonstrating good ruggedness characteristics. The high temperature measurement results showed that the breakdown voltage had little temperature dependence, which could be explained by a trap-assisted SCLC conduction model. With good breakdown ruggedness and reliability at high temperatures, the GaN p-i-n diodes grown on large-scale Si substrates exhibited promising potential for achieving cost-effective high-voltage rectifiers.

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